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Physics, modeling, and benchmarking of ULTRARAM: A compound semiconductor-based memory device

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Physics, modeling, and benchmarking of ULTRARAM: A compound semiconductor-based memory device

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ABSTRACT

ULTRARAM is a promising emerging memory exhibiting high endurance, long retention, and ultra-low switching energy per unit area. This compound semiconductor-based non-volatile memory utilizes triple barrier resonant tunneling (TBRT) through InAs/AlSb heterostructures. In this work, we have proposed a physics-based compact model of ULTRARAM memory device that captures the real-time trapping/de-trapping of charges in the floating gate and used to calculate the device characteristics. In addition, we have performed numerical simulations of the TBRT stack using the Schrödinger equation inside the quantum well with mono-layer (~ 0.6 nm) variations to check the impact on memory characteristics of the device. Array-level simulations and benchmarking highlight the promise of this technology.

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I. INTRODUCTION

Charge-based memories such as flash, dynamic random-access memory (DRAM), and static random-access memory (SRAM) are the primary contributors to the traditional memory market.¹ All these technologies have limitations, though.² Since it is non-volatile, flash memory has long been the favored option for data storage. Nevertheless, because of its high voltage requirements (≤ 20 V), flash has limited endurance.^{3,4} DRAM uses much lower voltages and runs faster than flash, but it has reached its limits of scalability, suffers from destructive reading operations, and requires data refreshing every ~ 60 ms, which increases energy consumption and degrades performance.^{5–7} SRAM is the fastest among all the charge-based memories available, although even for storing a single bit of data, it requires a large physical footprint (typically six transistors).^{8,9}

To tackle these challenges, a novel non-volatile memory technology known as ULTRARAM has been developed.^{10,11} Unlike traditional charge-based memories, ULTRARAM utilizes a non-classical charge-trapping mechanism, offering a unique combination of very low-energy consumption per unit area, excellent endurance, very robust non-volatility, and fast operation. To achieve these properties, ULTRARAM uses an InAs/AlSb TBRT process, explained in Sec. III. ULTRARAM integration onto Si substrates has also been demonstrated.¹¹ This is an important step toward large-scale fabrication due to superior mechanical characteristics and more environmentally sustainable production because of the plentiful supply of Si compared with group III and V elements. In this work, we have presented the device physics and a physics-based model to capture the device characteristics.

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This paper is arranged to discuss the details of the ULTRARAM memory concept in Sec. II. This is followed by the TBRT physics and ULTRARAM device modeling with benchmark in Secs. III and IV, respectively. We conclude in Sec. V.

II. MEMORY CONCEPT

ULTRARAM is a non-conventional charge-storage non-volatile memory (NVM) with a structure similar to flash but utilizes TBRT to achieve its remarkable properties, as shown in Fig. 1. Logic states are stored on a floating gate that is separated from the control gate (CG) by an oxide layer. The application of voltage on the CG results in the trapping of charges in the floating gate (FG) by a resonant tunneling process through the TBRT structure. The logic states (0/1) are determined by the presence/lack of charge on the FG. The non-destructive read process occurs by the application of voltage between the source (S) and drain (D). The novelty of ULTRARAM results from ultra-fast switching of the TBRT structure from a highly resistive state to a highly conductive state by applying a small voltage of ± 2.5 V. This is accomplished by careful design of the AlSb barrier and InAs quantum well (QW) layer thicknesses of the TBRT. Without applied voltage, the energy levels of the QWs reside at unusually high values, are not aligned with each other, and are well above the energy levels of the FG and channel layers, leading to a large barrier that prevents electron transfer into or out of the FG. This is a consequence of narrow QWs and the low electron-effective mass in InAs. However, the application of a positive bias to the CG tilts the conduction band in a way that the QW energy levels align with the occupied electron states in the channel, resulting in electrons flowing rapidly through the TBRT structure by intrinsically fast resonant tunneling into the FG (program). A negative bias on the CG has the equal and opposite effect (erase).

Molecular beam epitaxy was used to deposit the ULTRARAM layers on 3-in. Si n-type substrates. These substrates produce dia-

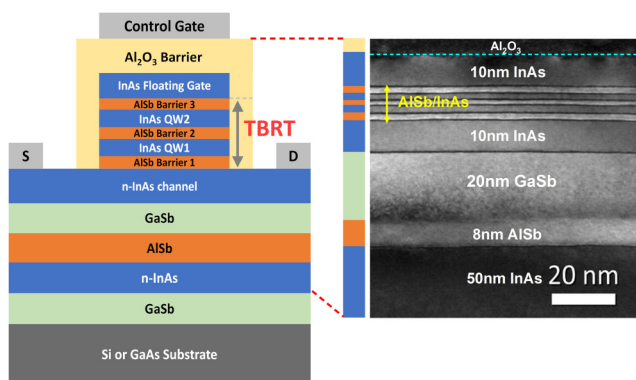


FIG. 1. Schematic of an ULTRARAM memory device and the corresponding TEM image.¹⁰ From Lane *et al.*, IEEE Trans. Electron Dev. **68**(5), 2271–2274 (2021). Copyright 2021 Author(s), licensed under a Creative Commons Attribution 4.0 (CC BY 4.0) license.

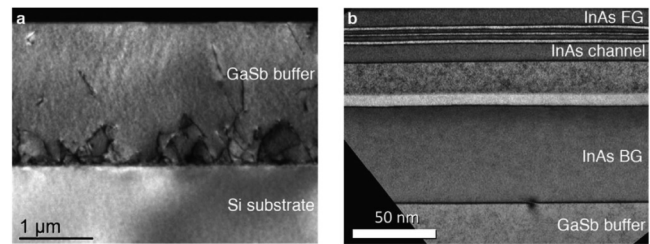


FIG. 2. III-V on Si material characterization. (a) Dark-field $g = 220$ transmission electron microscope (TEM) image of a GaSb/Si buffer layer. (b) Dark-field $g = 002$ TEM image of the ULTRARAM sample.¹¹ Only the memory layers and the top of the GaSb buffer are visible in this image. A single misfit dislocation is visible in the InAs/GaSb buffer interface. From Hodgson *et al.*, Adv. Electron. Mater. **8**(4), 2101103 (2022). Copyright 2022 Author(s), licensed under a Creative Commons Attribution 4.0 (CC BY 4.0) license.

pointing in the [011] crystal direction.¹² This feature aids in inhibiting the development of antiphase domains (APDs) in polar III-V materials as they grow. A GaSb buffer growth technique was developed in order to provide a high-quality III-V surface onto which the memory epilayers can be deposited. This was accomplished by first thermally desorbing the native oxide from the Si wafer's surface and then depositing a 17 monolayer (ML) AlSb nucleation layer, which resulted in the creation of 3D islands.¹³ These islands facilitated 2D epitaxy and minimized planar twinning defects by shortening the diffusion length of Ga atoms when depositing the subsequent $2\mu\text{m}$ GaSb buffer.¹⁴ An interface misfit array at the Si to III-V interface relieved the large lattice mismatch of 12.3%.¹⁵ A two-temperature-step GaSb growth process has been utilized to reduce the density of threading dislocations that spread vertically.¹⁶ The resulting GaSb buffer layer had a surface defect density of $(2.5 \pm 0.1) \times 10^8 \text{ cm}^{-2}$. TEM images in Fig. 2(a) showed that the buffer layer was APD free and the bulk of the threading dislocations was restricted to the first 500 nm of GaSb. This forms a high-quality, optimal GaSb buffer layer on the Si substrate that is

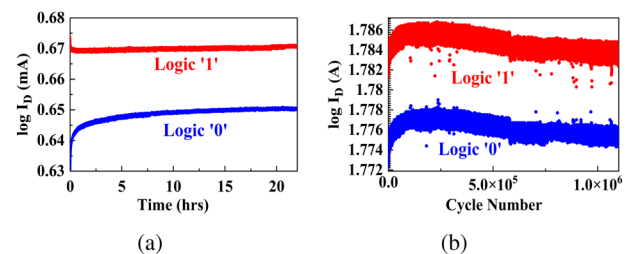


FIG. 3. (a) Room-temperature retention data. Program and erase cycles consisted of 10 ms duration pulses at ± 2.5 V. Readout is performed at an S-D bias of 0.2 V and in the absence of gate bias. (b) Endurance data for continuous program-read-erase-read cycling (5 ms pulses) on a memory cell demonstrating a clear 0/1 contrast exceeding 10^6 cycles.¹¹ From Hodgson *et al.*, Adv. Electron. Mater. **8**(4), 2101103 (2022). Copyright 2022 Author(s), licensed under a Creative Commons Attribution 4.0 (CC BY 4.0) license.

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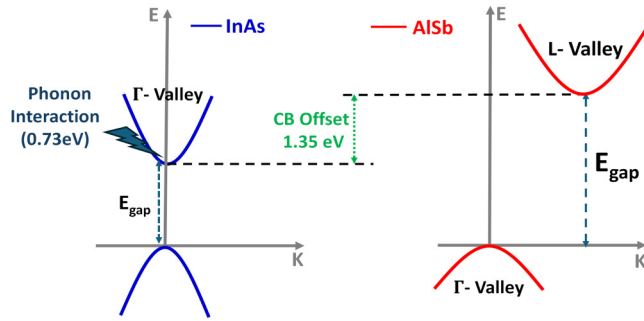


FIG. 4. Band structures of InAs (direct bandgap) and AlSb (indirect bandgap) as a function of wavevector (K).

appropriate for memory layer deposition. As seen in Fig. 2(b), the initial epilayers formed on this buffer are the 50 nm InAs n-type back gate (BG) and an 8 nm AlSb barrier layer. Next, a 20 nm GaSb spacer was deposited, followed by a 10 nm InAs n-type layer (channel) and the InAs/AlSb TBRT, which comprises 1.8 nm of AlSb, 3.0 nm of InAs, 1.2 nm of AlSb, 2.4 nm of InAs, and 1.8 nm of AlSb. Finally, the structure is completed by a 10 nm InAs FG. 10 and 20 μm devices were then fabricated using standard cleanroom techniques.¹¹ Figure 3 shows the measured retention and endurance characteristics of the ULTRAM memory cell on a Si substrate.

III. TBRT PHYSICS AND MODELING

Unlike flash, which uses a single SiO_2 barrier, ULTRAM utilizes a TBRT to store, charge, and discharge the FG. This structure provides a high-potential electron barrier (~ 2.1 eV) with no bias and allows fast resonant tunneling at program/erase pulse (± 2.5 V) with switching energy per unit area 1000 times lower than flash and 100 times lower than DRAM. InAs/AlSb have been chosen as QWs and barriers, respectively, resulting in high-quality heterojunctions due to the approximately matched lattice constant (6.1 Å). Also, this combination of materials provides a large conduction band offset of 1.35 eV. However, an additional phonon interaction of 0.73 eV is required to traverse the indirect bandgap of these materials, as shown in Fig. 4. Consequently, the conduction band offset of the InAs/AlSb heterojunction forms a 2.1 eV

energy barrier for electron transport. We have performed numerical simulations of the TBRT stack using the Schrödinger equation inside the QW with mono-layer (~ 0.6 nm) variations,¹⁷ as given in Table I. Figure 5 shows the variations in the QWs and barrier thicknesses and their corresponding change in the energy levels and probability density of wave functions. Additionally, the impact of energy level changes on the current density of the TBRT stack is shown in Figs. 6(a) and 6(b), as well as the change in the memory window of the device is shown in Figs. 6(c) and 6(d). This shows notable differences when the QW widths are varied, as the changes in energy levels are significant. However, a very minute change has been seen with the change in barrier thickness, as the resonant tunneling mechanism is still the same with ± 1 ML barrier change, and the same can be observed in Fig. 5. TBRT parameters are, thus, sensitive to a 0.6 nm monolayer variation in the QWs, which would lead significant changes in the device characteristics. This highlights the requirement for precise control of QWs during fabrication, as these are more critical to stabilize the device characteristics. Further work is required to assess variations in fabrication and changes in material properties at sub-nanometer nodes.

To capture the trapping/de-trapping in the FG through the TBRT barrier, we have developed a physics-based compact model for multi-barrier resonant tunneling current.¹⁸ The compact model assumes that (a) the tunneling process preserves the transverse momentum, (b) the distribution of the electric field is uniform in the structure, and (c) the effective mass approximation.¹⁹ Using these, the current density can be described as¹⁸

$$J = \frac{q_e m^* k T}{2\pi^2 \hbar^3} \int_0^\infty T(E_x, V) D(E_x, V) dE_x, \quad (1)$$

where q_e is the charge of an electron, m^* is the effective mass of the electron, k is Boltzmann's constant, T is the absolute temperature, $\hbar$ is reduced Planck's constant, E_x is the longitudinal energy, V is the potential applied to the structure, and $D(E_x, V)$ is the supply function and can be given as

$$D(E_x, V) = \ln \left[\frac{1 + \exp\left(\frac{E_f - E_x}{kT}\right)}{1 + \exp\left(\frac{E_f - E_x - q_e V}{kT}\right)} \right]. \quad (2)$$

TABLE I. Monolayer thickness change in TBRT stack.

ML change	AlSb B1 (nm)	InAs QW1 (nm)	AlSb B2 (nm)	InAs QW2 (nm)	AlSb B3 (nm)
Ref. layer	1.8	3.0	1.2	2.4	1.8
+1 ML QW	1.8	3.6	1.2	3.0	1.8
-1 ML QW	1.8	2.4	1.2	1.8	1.8
+1 ML barrier	2.4	3.0	1.8	2.4	2.4
-1 ML barrier	1.2	3.0	0.6	2.4	1.2

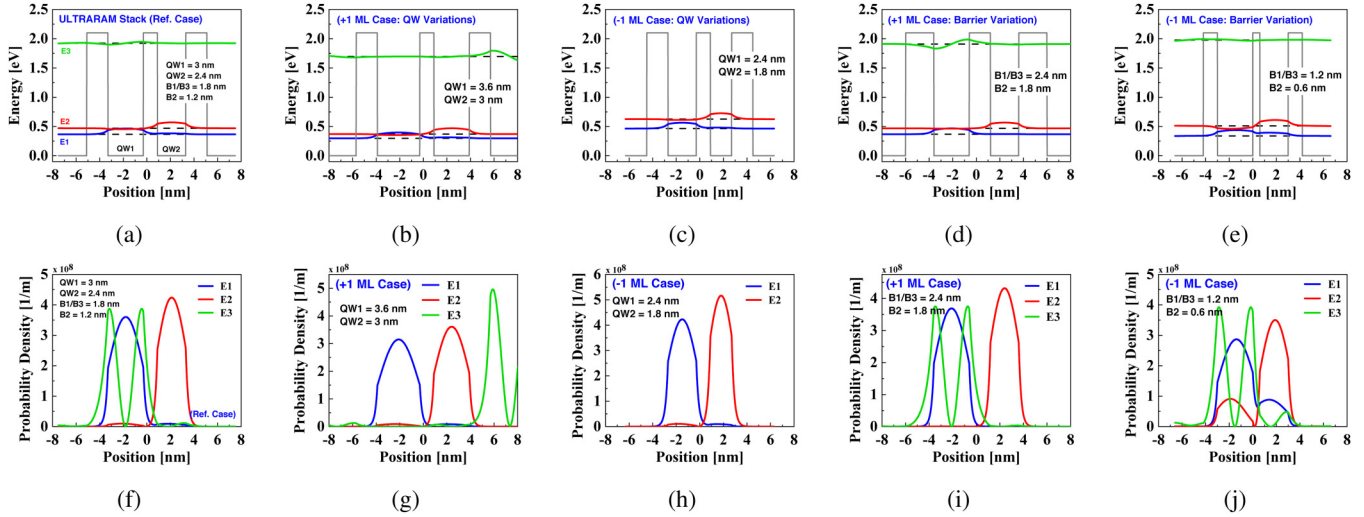


FIG. 5. The TBRT quantum well wave functions and energy levels for (a) the ULTRARAM memory (reference case), (b) and (c) ± 1 ML change in QW thicknesses, and (d) and (e) ± 1 ML change in barrier thicknesses. Variations in probability density (f) for ULTRARAM memory (reference case), (g) and (h) ± 1 ML change in QW thicknesses, and (i) and (j) ± 1 ML change in barrier thicknesses.

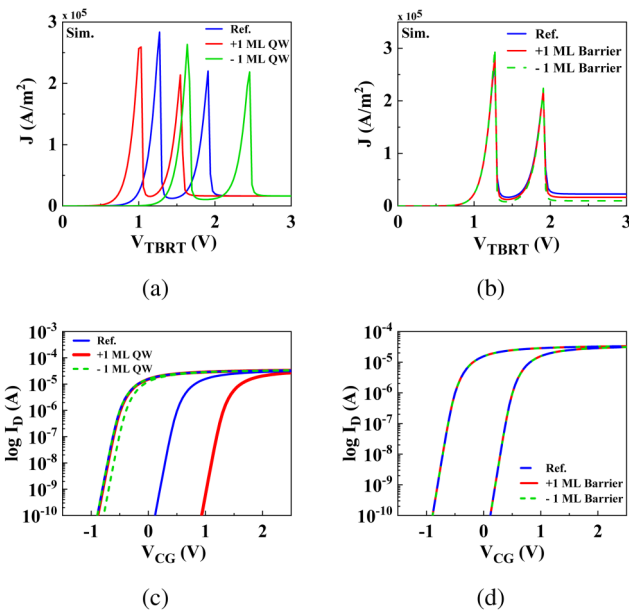


FIG. 6. Change in the TBRT current density with mono-layer (ML) change in (a) QWs and (b) barrier thicknesses with respect to TBRT stack voltage (V_{TBRT}). Change in memory window of the device with a ML change in (c) QWs and (d) barrier thicknesses of TBRT stack with respect to control gate voltage (V_{CG}). Here, ± 1 ML is the change in one lattice constant (0.6 nm) as specified in Table I.

$T(E_X, V)$ is the tunnelling transmission coefficient approximated as¹⁹

$$T(E_X, V) = \frac{\Gamma^2}{(E_X - (E_R - q_e Vn))^2 + \Gamma^2}, \quad (3)$$

where Γ is the half-width of resonance level, E_R is the energy of the resonant level relative to the bottom of the well at its center, and n is the voltage drop factor at the center of the well. For equal width barriers, n is 0.5; otherwise, it can be determined from the analysis or used as a fitting parameter. $T(E_X, V)$ is assumed to be Lorentzian, and it is negligible if Γ is small compared to thermal energy (i.e., $E_X = E_R - q_e Vn$). Now, solving the integration in Eq. (1) using Eqs. (2) and (3) results in the resonant tunneling current density for the double barrier and can be given as

$$J = J_0 D(E_X, V) \left[\frac{\pi}{2} + \tan^{-1} \left(\frac{E_R - q_e Vn}{\Gamma} \right) \right], \quad (4)$$

where $J_0 = q_e m^* kT / (2\pi^2 \hbar^3)$.

$$J_{tbrt} = J_0 \ln \left[\frac{1 + \exp\left(\frac{E_f - E_{R1} + q_e Vn_1}{kT}\right)}{1 + \exp\left(\frac{E_f - E_{R1} + q_e V(n_1 - 1)}{kT}\right)} \right] \left[\frac{\pi}{2} + \tan^{-1} \left(\frac{E_{R1} - q_e Vn_1}{\Gamma_1} \right) \right] \\ + J_0 \ln \left[\frac{1 + \exp\left(\frac{E_f - E_{R2} + q_e Vn_2}{kT}\right)}{1 + \exp\left(\frac{E_f - E_{R2} + q_e V(n_2 - 1)}{kT}\right)} \right] \left[\frac{\pi}{2} + \tan^{-1} \left(\frac{E_{R2} - q_e Vn_2}{\Gamma_2} \right) \right] \\ + H \left(e^{q_e Vn_3 / kT} - 1 \right). \quad (5)$$

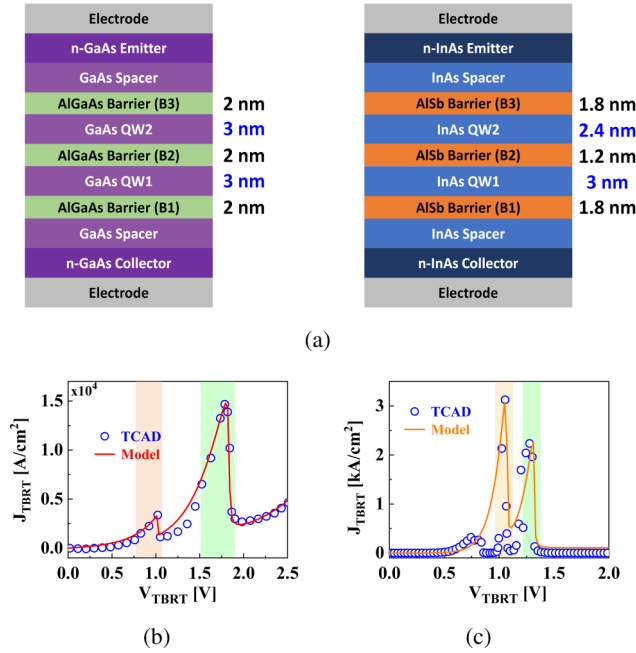


FIG. 7. Schematic of (a) GaAs/AlGaAs and InAs/AlSb material-based TBRT structures used for TCAD simulations. (b) and (c) Validation of the proposed model with TCAD data.

In the TBRT, there are two resonance levels. The second resonance in the TBRT can be modeled using an additional term similar to Eq. (4). This form produces the double peaks due to resonant tunneling. To capture the thermal excitation over a barrier, an additional thermionic component can be added as $J_{th} = H(e^{eV_{n3}/kT} - 1)$, where H and n_3 can be used as fitting parameters. Equation (5) shows the current density for the TBRT stack. This accurately captures the TBRT current density and has been validated with two different compound semiconductor-based TBRT stacks, as shown in Fig. 7.

We have simulated the TBRT structure in a commercial TCAD simulator, where the self-consistent Poisson-Schrödinger equation and the non-equilibrium Green's function (NEGF) approach are used. The NEGF model, which considers the fluctuation properties of electrons in the direction of transport and transverse, can be used to predict eigen energies, eigenfunctions, and current-voltage characteristics of the QW. In particular, we have validated the model of Eq. (5) with AlSb/InAs-based TBRT used in ULTRARAM devices, where AlSb is the barrier material and InAs is the QW. Note that there is a negligible contribution of thermionic current at room temperature.

IV. ULTRARAM MODEL AND BENCHMARKING

The current density from the TBRT model is further used to calculate charge trapping and de-trapping in the FG of ULTRARAM. An R-C network has been used to integrate the TBRT current over the applied input duration to obtain the real-

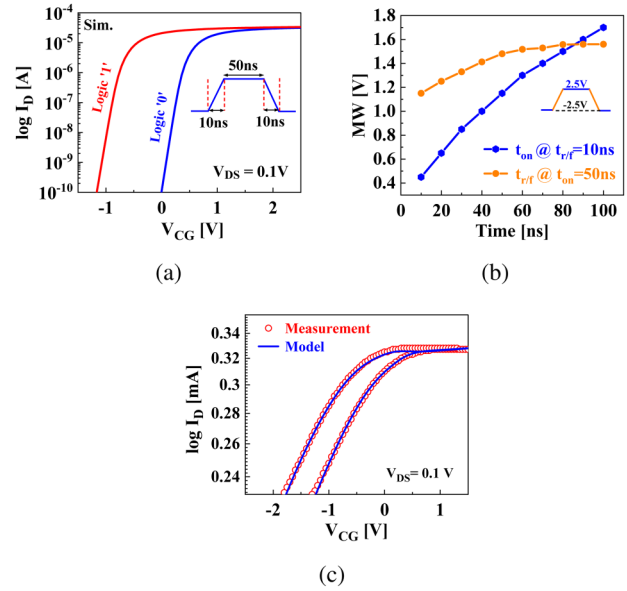


FIG. 8. (a) Simulated I-V with the applied input gate pulse of $\pm 2.5V$, $L_g = 1\mu m$, and $W = 1\mu m$. The gate capacitance $C_{gg} \approx 7fF$ has been calculated using the model. (b) Variations in MW of the device for pulse width (t_{on}) and rise/fall time (t_r/t_f) of the input gate pulse. (c) Validation of model with experimental I-V characteristics.¹¹ The following parameters have been used for calibration: $L_g = 10\mu m$, $W = 17\mu m$, and voltage pulse of $\pm 2.5V$. The $C_{gg} \approx 1.2pF$ has been calculated using the model.

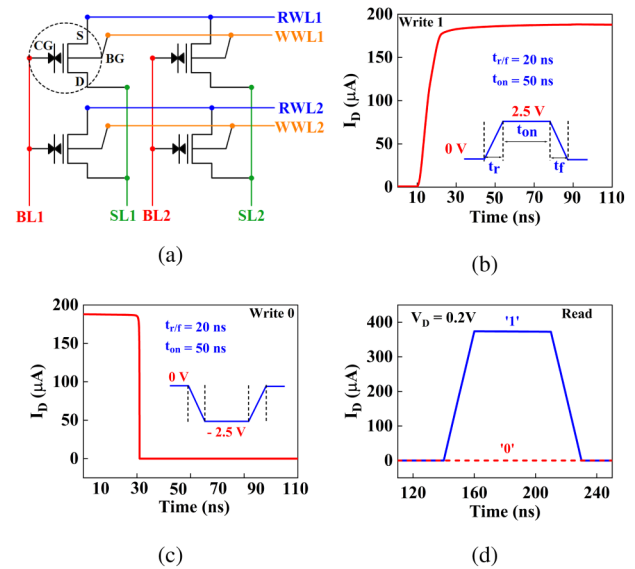


FIG. 9. (a) 2×2 Array with ULTRARAM memory cells, (b) Write "1" operation, (c) Write "0," and (d) Read operation.

TABLE II. Biasing scheme for a specific ULTRARAM cell.

Memory Operation		Write (V)	Read (V)
WWLs	Accessed	0	0
	Others	$V_{WRITE}/2$	0
RWLs	Accessed	0	V_{READ}
	Others	0	0
BLs	Accessed	V_{WRITE}	0
	Others	$V_{WRITE}/2$	0
SLs	Accessed	0	0
	Others	0	0

time FG charge. Furthermore, this charge is used to calculate the threshold voltage shift in the program/erase state. The drain current of the device can be expressed as

$$I_{ds} = \mu_{eff} C_g \frac{W}{L} \left(V_{gs,eff} - V_{off} - \frac{Q_{FG}}{C} - \psi_m \right) \psi_{ds}, \quad (6)$$

where μ_{eff} is the effective mobility, C_g is the gate capacitance, W is the device width, L is the channel length, $V_{gs,eff}$ is the effective applied gate voltage, V_{off} is the cut-off voltage, Q_{FG} is the charge in the FG, and ψ_{ds} is the drain to source surface potential. $\psi_m = (\psi_s + \psi_d)/2$, where ψ_s and ψ_d are the surface potentials at the source and drain side, respectively. ψ_s and ψ_d were calculated as given in Ref. 20.

Figure 8(a) shows the $I_d - V_{gs}$ results simulated from the model for the programmed and erased states. The memory window (MW) depends on the input waveform, which is accurately captured in real time by the proposed model. Variation with pulse width (t_{on}) and rise/fall time ($t_{r/f}$) is shown in Fig. 8(b). We have also validated the model with experimental data of ULTRARAM, as shown in Fig. 8(c). The model shows excellent accuracy. This work focuses on demonstrating device characteristics and model validation for single-level cell operation. However, owing to ULTRARAM using a floating gate structure similar to flash, there is the possibility of controlling the amount of charge injected into the floating gate. Different numbers of charges can be stored in the floating gate by the application of gate pulses with different widths

and amplitudes. This would enable the feasibility of multi-level cell operation by modulating the threshold voltage of the device in intermediate steps rather than just the two levels studied here.

A 2×2 memory array, as shown in Fig. 9(a), is evaluated. The array includes distinct read–write paths, preventing accidental changes to stored states. Additionally, our design enables reading all cells in a column with a single cycle without scalability constraints. Moreover, the read operation is independent of the write mechanism, providing flexibility to optimize the read process for both memory and in-memory computing applications. To perform the write operation in any specific cell, the write voltage (V_{WRITE}) has been applied between the control gate and back gate of the cell using the bit lines (BLs) and write word lines (WWLs). During the read operation, we apply the read voltage between the source (S) and drain (D) of the cell through the sense line (SL), maintaining the control gate voltage (V_{CG}) at 0 V. The SL current depends on the difference in the S–D current level. To prevent any accidental write, the V_{SD} should not exceed $V_{WRITE}/2$. Table II shows the biasing schemes for the read and write operation for a ULTRARAM cell. Figures 9(b)–9(d) show the write 0/1 and read operation of the accessed cell. Table III shows the performance comparison of the ULTRARAM cell with other memory cells. ULTRARAM has the ability to bridge the gap between last-level cache and storage-class memories in the memory hierarchy,²⁵ owing to its latency and capacity, and can outperform NAND flash in specific areas such as speed, endurance, and energy. Therefore, it can complement NAND flash technology to achieve a better hybrid memory system with overall better performance.

Here, we have primarily focused on the device design and a physics-based compact model of single ULTRARAM cells to capture core device characteristics. However, it is understood that the real performance metrics should be judged by large array-level demonstration. We have also simulated a 128×128 array of ULTRARAM cells using the proposed model. A circuit-level macro-model is employed to evaluate and benchmark the on-chip learning performance in terms of area, latency, energy, and accuracy of an ULTRARAM synaptic core. It shows 91% accuracy for ULTRARAM-based CIM accelerators for VGG-8 training on the CIFAR-10 dataset, which is similar to NAND Flash-based CIM accelerators ($\sim 90\%$) with 5-bit weight.²⁶ Full details will be disseminated in a separate article.

TABLE III. Performance metrics of ULTRARAM with other memory technologies.

Metric	SRAM ²¹	DRAM ^{21,22}	Flash ²¹	Fe-RAM ²³	STTRAM ^{22,24}	ULTRARAM (this work)
Cell area (F ²)	>100	6	<4	15–35	6–50	<4
Voltage (V)	<1	<1	>10	<5	<1.5	<2.5
Switching energy (J)	10^{-15}	10^{-15}	10^{-14}	10^{-11}	10^{-13}	10^{-17}
Retention	40 ms	60 ms	>10 years	>10 years	>10 years	>1000 years
Endurance	10^{16}	10^{16}	10^4	$>10^{10}$	10^{14}	$>>10^{7a}$
Switching time (ns)	1	10	10^5	20	~ 50	$\sim 100^b$

^aExperiment limited. Zero degradation observed after 10^7 program/erase cycles.

^b100 ns switching time has been observed in TCAD simulations for 20 nm channel length devices. The experimental device shows 500 μ s switching time with 20 μ m channel length.¹⁰

V. CONCLUSIONS

A compact model for ULTRARAM is presented providing a clear and uncomplicated physical basis for its extraordinary properties and allowing circuit-level benchmarks. The model is able to capture real-time device characteristics and shows excellent accuracy with both TCAD and measured data for TBRT and ULTRARAM, respectively. This SPICE-compatible model has been implemented in Verilog-A and is directly usable for circuit analysis.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Abhishek Kumar: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Software (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Musaibh Farooq Dar:** Data curation (equal); Formal analysis (supporting); Software (supporting); Visualization (equal); Writing – original draft (supporting). **Peter D. Hodgson:** Data curation (equal); Formal analysis (equal); Investigation (equal); Project administration (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – review & editing (equal). **Dominic Lane:** Formal analysis (supporting); Project administration (equal); Validation (equal); Visualization (equal); Writing – review & editing (equal). **Peter J. Carrington:** Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – review & editing (equal). **Evangelia Delli:** Data curation (equal); Formal analysis (equal); Investigation (equal); Validation (equal); Visualization (equal); Writing – review & editing (equal). **Richard Beanland:** Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Resources (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – review & editing (equal). **Shruti Mehrotra:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – review & editing (equal). **Manus Hayne:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing –

original draft (equal); Writing – review & editing (equal). **Avirup Dasgupta:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Resources (equal); Software (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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