QuInAs Technology

ULTRARAM™

ULTRA-EFFICIENT MEMORY

High-performance – Non-volatile

Universal Memory

"Powering Future Compute & AI"

TAIWAN CHIP-BASED INDUSTRIAL INNOVATION PROGRAM

Most Innovative Memory Technology

ELEKTRA 2023

TechWorks

TechNES

WIPO

James Ashforth-Pook

Co-founder & CEO - Quinas Technology Ltd.

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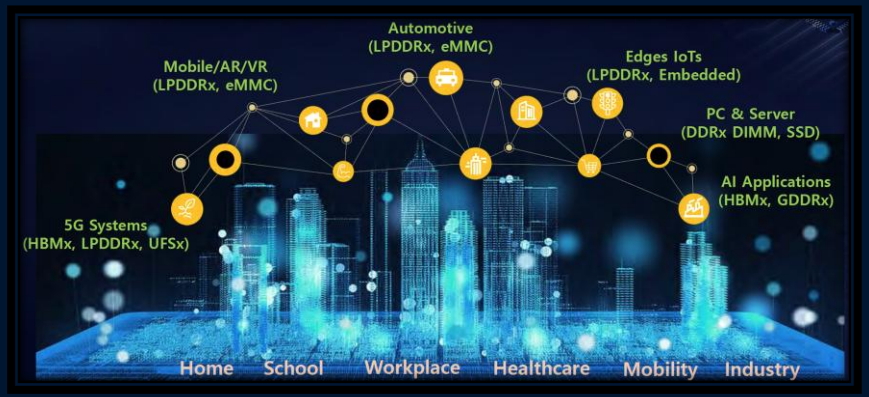
250705v2

Memory Growth Engine

Explosive growth ahead: AI to drive $1T market by 2030



Memory powers every sector - from edge to cloud

ULTRARAM™ is uniquely positioned to meet this need

Legacy Memory Cannot Power the Future

Why the world urgently needs a breakthrough memory technology

🔋 Digital Energy Pressure

- Data centres consume 2–3% of global electricity
- Projected to double by 2030
- DRAM's constant power draw is a core inefficiency

⚙️ Performance vs. Power Trade-Off

- AI, 5G/6G, and Edge workloads need memory that is:
  - Fast, Non-volatile, and Energy-efficient
- No current memory tech achieves all three

🚧 Industry at a Scaling Wall

- Moore's Law and Denard Scaling are breaking down
- DRAM: fast but volatile and power-hungry
- NAND: non-volatile but slow, with limited endurance

📉 Market Gap = Investor Opportunity

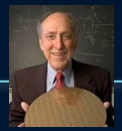
- $150B+ memory market is ripe for disruption
- Legacy memory can't meet sustainability goals
- A new memory class is needed to unlock growth

ULTRARAM™ is designed to break the speed–power–volatility deadlock and redefine the future of memory.

Solution - ULTRARAM™

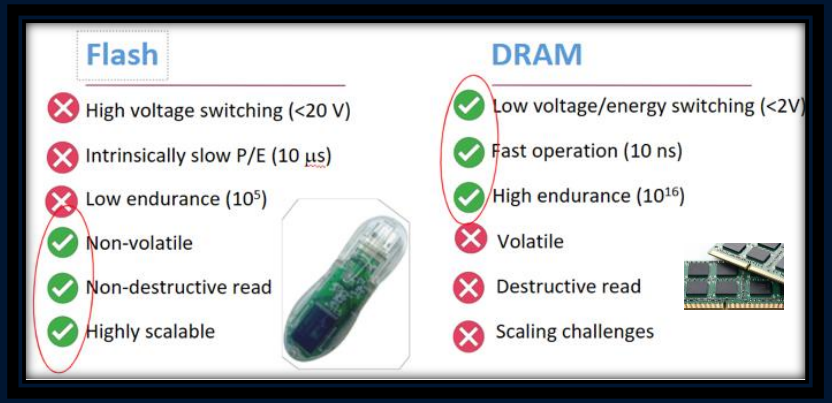
1980

TOSHIBA



1966

IBM

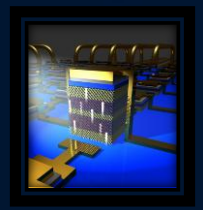


- Flash is non-volatile, but slow and wears out...
- DRAM is fast, but volatile and inefficient due to constant refreshing

What is the ULTRARAM™ Breakthough?

- A revolutionary universal memory combining:
  - Non-volatility of flash.
  - Speed and endurance beyond DRAM.
- Ultra-low power consumption for sustainable data processing.

Core Technology:



- Compound semiconductors replace silicon for enhanced performance. (InAs/GaSb-based quantum wells)
- Triple-barrier resonant tunneling **(TBRT)** eliminates refresh cycles, wear issues and drastically reduces power.

ULTRARAM™ combines the speed of DRAM with the persistence of Flash — without their flaws.

Defensible Disruptive Innovation

Patented Physics Breakthroughs:

- Anchored by our proprietary Triple Barrier Quantum Resonant Tunneling **(TBRT)** technology, enabling unprecedented energy efficiency and performance.
- Protected by multiple global **PATENTS** (2014>) across the
  - US, UK/Europe, Japan, South Korea & China.

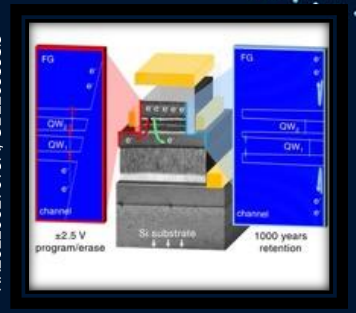
Advanced Materials and Design:

- Incorporates compound semiconductors like **InAs, GaSb, and AlSb** for unmatched endurance and efficiency.
- Scalable to silicon substrates, ensuring compatibility with existing fabrication ecosystems to accelerate adoption.

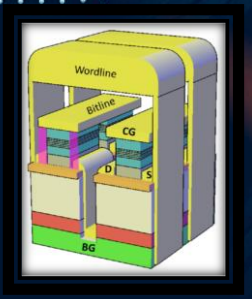
Award-Winning Innovation:

- **Winner of "Most Innovative Startup"** at the Flash Memory Summit 2023 USA.
- **Winner IC Taiwan Grand Challenge 2024** together with a $3m SAFE note option
- **WIPO Global Awards 2025** spinouts that leverage Intellectual Property backed innovation and creation in an exceptional manner

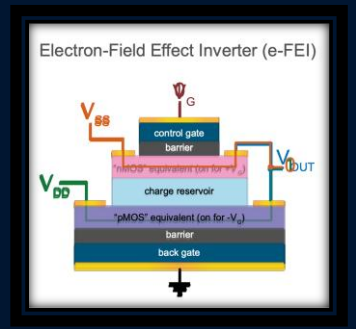
* US10243086B2, US17614813, EP3977457A1, CN114080682A, JP2022536268A, KR20220027079A, GB2209395.9



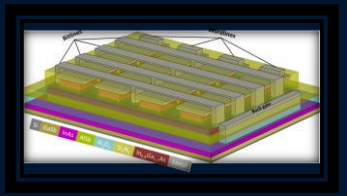
Memory Device Physics



Scalable Bit Cell



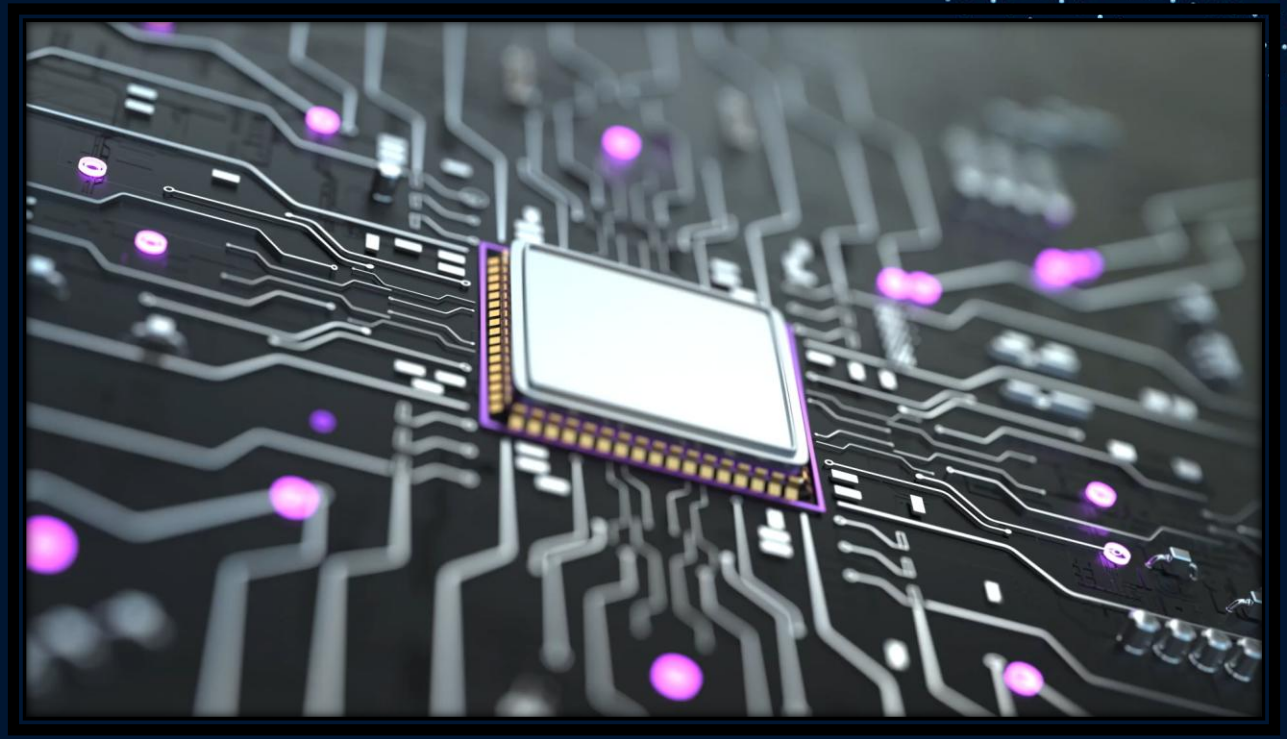
Logic Device



Memory Array

16-bit RAM array design @ 4F2

Explainer Video



https://bit.ly/ultraram

Unparalleled Performance

Performance Highlights (20nm Node):

- **Switching Energy**: 10 attojoules – 100x lower than DRAM and 1,000x lower than NAND.
- **High Endurance**: >10^{16} cycles, exceeding DRAM and other emerging memories.
- **Speed**: Switching time of ~1ns, faster than DRAM.
- **Non-Volatility**: Data retention >1,000 years, ideal for critical systems.
- **Wide Temperature Range**: Operates reliably in extreme conditions, exceeding 150/200°C.
- **Radiation Hardness**: Designed for harsh environments, including space and defense applications.

Energy Efficiency: Drastically reduces power requirements for memory-intensive applications.

NV >1k yrs

Super Fast

High endurance

Low disturb

Ultra-efficient

Wide temp range

RadHard

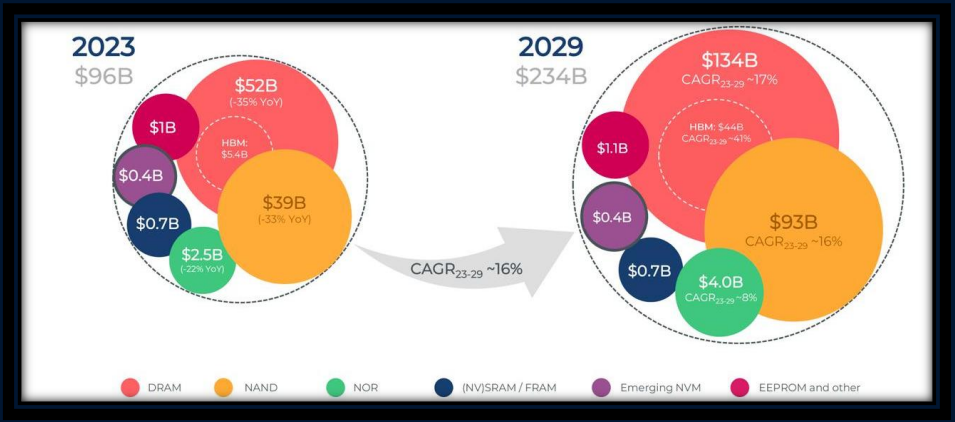
Benchmarking (projected 20 nm node)

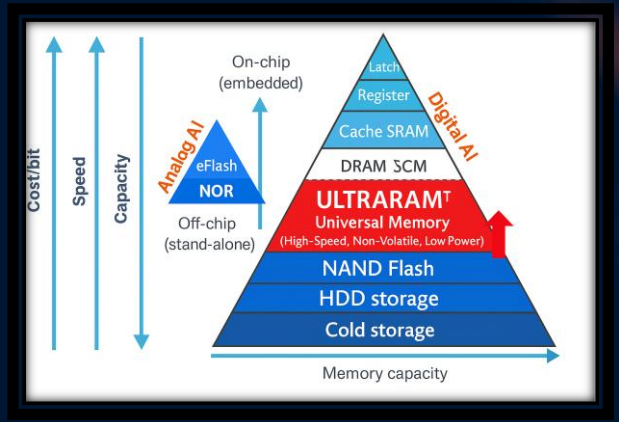
Parameter	DRAM	3D NAND	MRAM	ReRAM	PCRAM	ULTRARAM™	
Storage time	~60 ms	>10 years	>10 years	> 10 years	>10 years	**>10 years**	●
Non-destructive read?	No	Yes	Yes	Yes	Yes	**Yes**	●
Switching energy	1 fJ	~10 fJ	~100 fJ	~1,000 fJ	>1 pJ	**~10 aJ(*)**	●
Switching voltage	<1 V	>10 V	<1.5 V	<3 V	1-3 V	**≤2.5 V**	○
Energy barrier	0.5 eV	1.6 eV	1.5 eV	1.4 eV	2.4 eV	**2.1 eV**	●
Cell size	$6F^2$	$<<4F^2$	$6F^2$	$(4\text{-}12)F^2$	(4-30)	**$\leq 6F^2$**	●
Switching time	10 ns	>10 ms	10-50 ns	10-100 ns	10-100 ns	**~1 ns(*)**	●
Endurance	10^{16}	10^5	10^{12}	Up to 10^{12}	Up to 10^{12}	**$>10^{16}$ (**)**	●

(*)Current devices are at 10 μm node, which limits speed and increases switching energy by a factor of ~10^6

(**)Current measured endurance is experiment not device limited

$234B Memory Opportunity





South Korea

USA

Taiwan

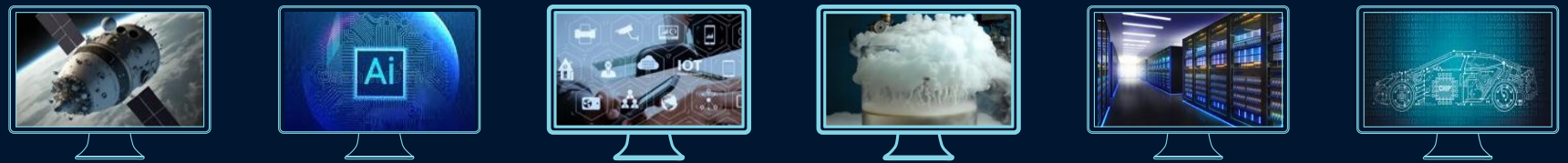
Japan

ULTRARAM™
The future of memory fast, persistent, and ready to replace DRAM

Addressable Markets and Applications

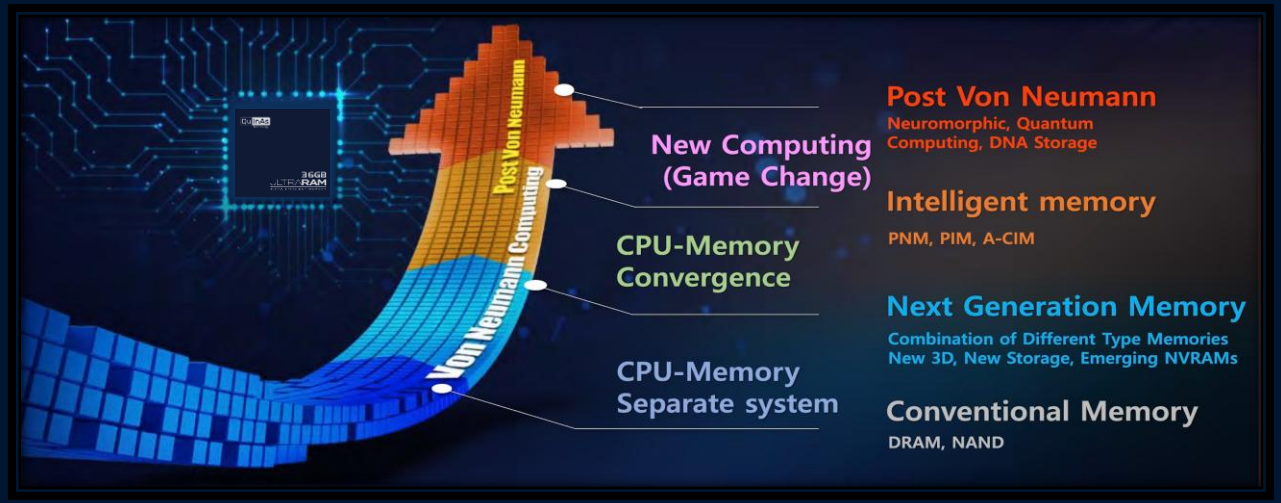
Core Markets:

- **Space & Defence**: Radiation-resistant, ultra-reliable memory for extreme environments.
- **AI and Edge Computing**: Enhances in-memory compute for low-latency AI tasks.
- **Data Centers**: Delivers significant energy savings in large-scale storage and processing.
- **Telecoms**: High-speed, energy-efficient memory for 5G/6G infrastructure.
- **IoT Devices**: Extends battery life and boosts performance for consumer electronics.
- **Automotive**: Supports advanced systems with extreme temperature resilience and reliability.



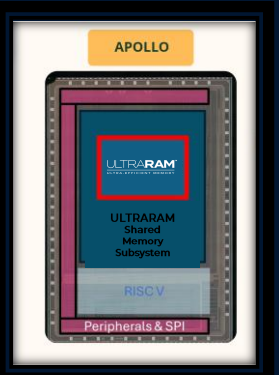
Future Memory-Centric Technology Directions

- Starting from DRAM and NAND, memory will continue to take various paths by evolving functional traits



ULTRARAM™
ULTRA-EFFICIENT MEMORY

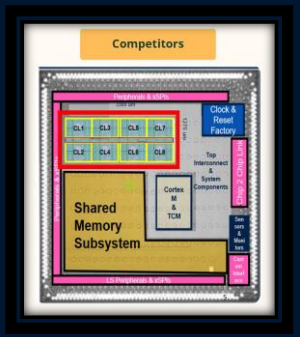
Revolutionising Compute with Analog In-Memory Processing – “MVAP”



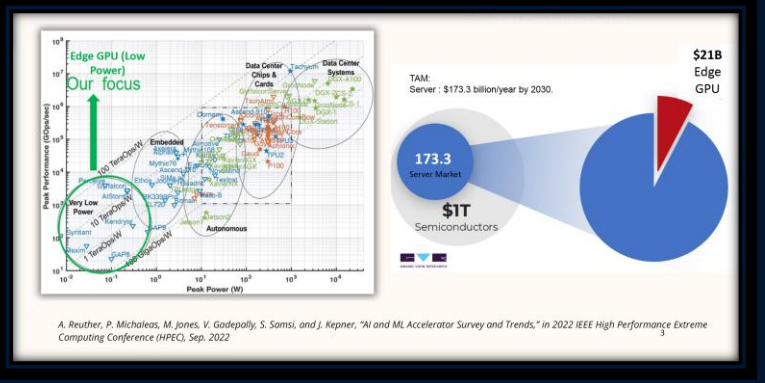
MAJOR DIFFERENCE
Memory Integration

Competitors use Digital SRAM and separate analog RRAM storage;

Our design is a bottom-up approach in which we combine analog ULTRARAM for Compute and storage using proprietary peripherals



ULTRARAM™
is transforming the memory landscape — offering unparalleled performance, energy efficiency, and scalability for next-generation applications



A. Reuther, P. Michaleas, M. Jones, V. Gadepally, S. Samsi, and J. Kepner, “AI and ML Accelerator Survey and Trends,” in 2022 IEEE High Performance Extreme Computing Conference (HPEC), Sep. 2022

DiRac Lab
ECE, IIT Roorkee

Literature	Die Layout	Type	Efficiency (TOPS/W)	Density (TOPS/mm2)	Array Size	ADC Type
BM LABS		RRAM-CMOS	30 (8 levels)	0.29	128X128X2	TDC
ULTRARAM		Floating Gate	80 (32 Levels)	~0.29 (6F2)	Development	TDC
NVIDIA H100		Full-CMOS	9.36	0.04 (400F2)	-	-
Google TPU v1		Full-CMOS	2.3	0.06	-	SAR
PUMA		RRAM-CMOS	0.42	0.29	128 × 128	SAR
3D-aCortex		RRAM-CMOS	70.4	0.58	64 × 128	Temporal to digital

Outperforming DDR5 in Power, Performance & Potential

Validated by ETH Zurich SAFARI Group

ETH zürich

SAFARI

Modelling by ETH Zürich (SAFARI Lab) predicts disruptive gains in efficiency and scalability.

Why ULTRARAM™ Stands Out:

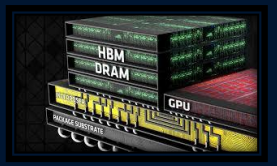
Combines the strengths of DRAM and NAND without their weaknesses.

Sustainable: Reduces energy consumption by orders of magnitude addressing the data centre energy crisis.

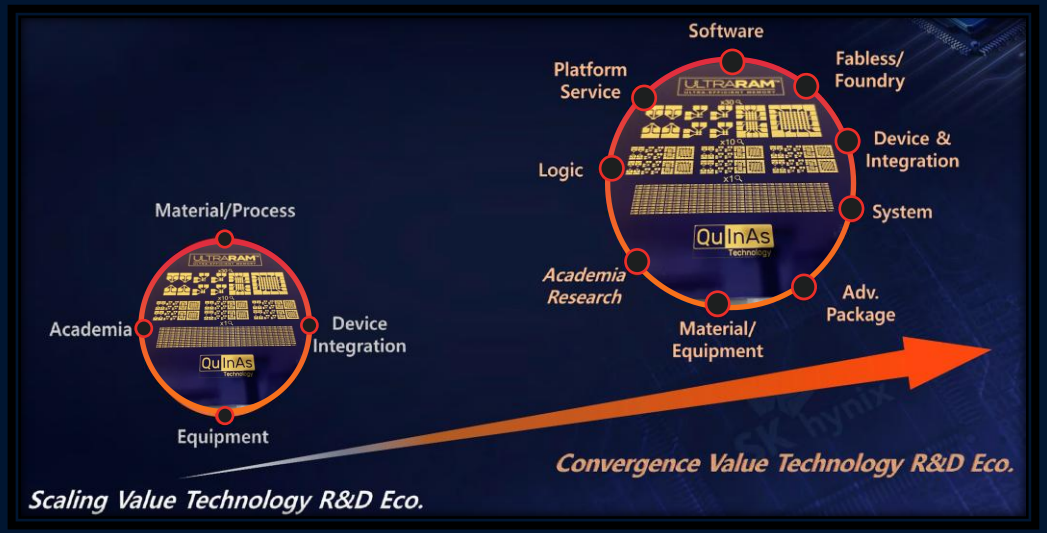
Scalable: Designed for seamless integration into existing global manufacturing systems.

Reliable: Long retention, high endurance, and radiation resistance for mission-critical use cases..

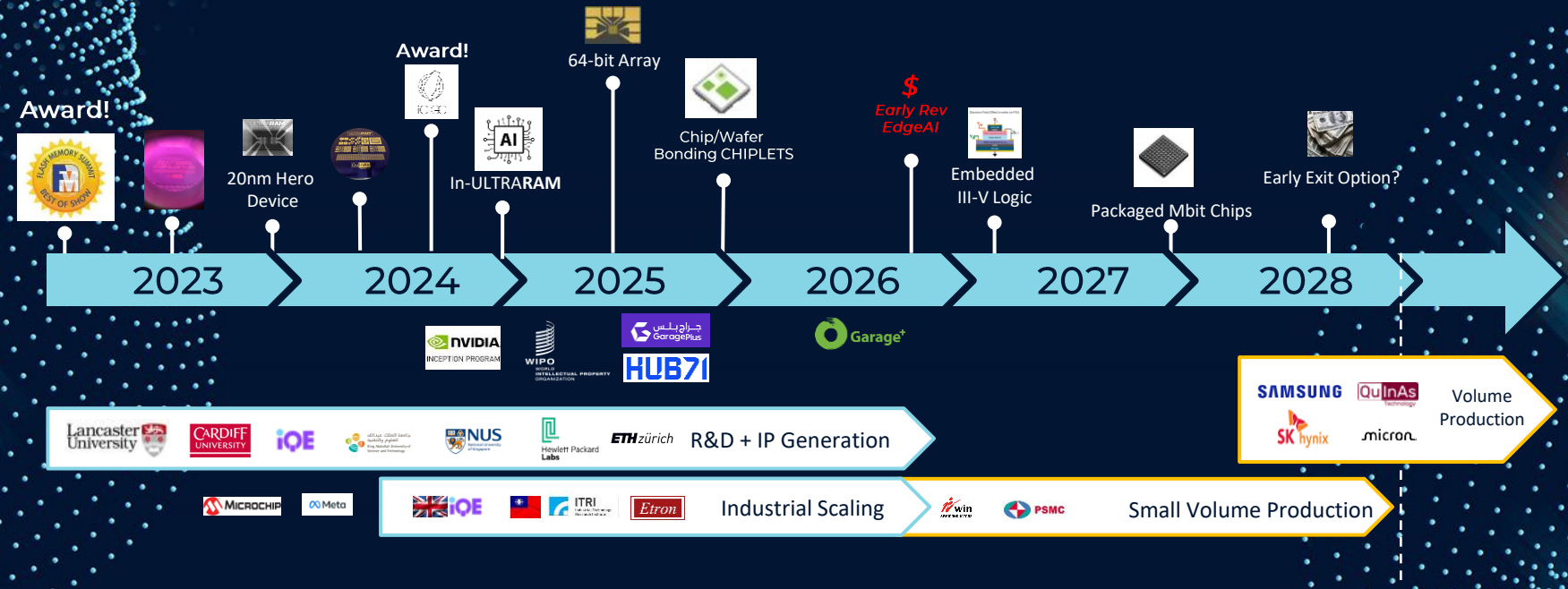
Future Proof: Positioned for future computing paradigms, including AI, neuromorphic and the secure quantum-era systems.



Collaboration is Driving our Innovation!



Roadmap to Commercialisation



2025: Develop pilot-scale 64-bit array and integrate packaging solutions for Edge AI applications.
2026: Begin small-volume production and explore early adopter markets (telecom, space).
2027: Commercialise packaged memory chips and launch advanced packaging (chiplets).
2028+: Scale to volume production and target widespread adoption in telecoms, data centers, and IoT.

Industrial Epitaxy of ULTRARAM™

Quinas Technology, IQE plc, Lancaster University, and Cardiff University are collaborating to advance ULTRARAM's technology readiness level (TRL) from 4 to 5 by scaling epitaxy from 3" wafers using molecular beam epitaxy (MBE) at Lancaster University to 6" wafers via metal-organic chemical vapour deposition (MOCVD) at IQE.

- Quinas Technology leads the project, with IQE focusing on epitaxy scale-up, Cardiff University providing MOCVD support, and Lancaster University handling fabrication and testing.
- This initiative represents a breakthrough in next-generation memory technology with significant commercial potential.

- This 12-month project, **£1M+** funded by Innovate UK under the Scaling-up Semiconductor Manufacturing – CR&D competition, aims to establish industrial viability for ULTRARAM.
    - ***Key goals include scaling up production with industrial tools, fabricating and testing memory devices.***
- With a £355k investment from IQE, this initiative presents a significant opportunity for IQE to enter the $165bn memory sector, challenging silicon-based incumbents and securing future wafer supply for large-scale ULTRARAM production.

The project will facilitate investment and commercialisation, positioning Quinas as a disruptive force in the memory market.

Team Expertise

Founder team

James Ashforth-Pook
CEO
38+ years in high-growth startups and semiconductors.

Prof Manus Hayne
CSO
inventor of ULTRARAM™ and quantum tunneling expert.

Dr Peter Hodgson
CTO
specialist in device scaling and fabrication.

Research team

Dr Serdar Tekin
Postdoc
(arrays)

Jono Hall
PhD
(logic)

Bianca Giuroiu
PhD

Xiuxin Xia
PhD
(scaling)

Kacper Burczyk
PhD

External Tech advisors

Dr J. Iwan Davies
Grp Tech Dir, IQE PLC

Dr Pierre Fazan
IMEC Fellow/Micron Technology

Prof Avirup Dasgupta
Indian Institute of Tech Roorkee

Recruiting additional advisors from the UK, India, South Korea and the USA

*Global Collaboration Network: Partnerships with: IQE, CU, IIT-R, ETH-Z, NUS, KAUST.

Global Achievements

·2019: 2nd most accessed physics and 41st most accessed paper overall in Scientific Reports (>26k)
·2019: First patent awarded (US10243086B2)
·2022: Paper makes issue back cover and editor's choice as best of the year in Advanced Electronic Materials
·**Feb 2023: Quinas formally incorporated in England & Wales UK**
·Mar 2023: ICURe pitch panel recommended spinout
·Aug 2023: **'Most Innovative Startup' award, Flash Memory Summit, Silicon Valley**
·Aug 2023: Selected for the Octopus Ventures "Springboard" - game changing, sustainable technologies
·Sep 2023: Department of Business and Trade (DBT) mission to **TAIWAN** (sponsored by Innovate UK)
·Oct 2023**: £300k ICURe Innovate UK project commenced**
·Oct 2023: Selected by DSIT to join the ChipStart UK Incubator Accelerator program
·Nov 2023: Finalist for PraxisAurilKE 'Commercialisation Achievement of the Year'
·Nov 2023: Winner Elektra Reader's Choice Award 'University Research Group of the Year'
·Dec 2023: Finalist TechWorks' TechNES Design Award'
·Dec 2023: Visit by Prof Julia Sutcliffe, Chief Scientific Advisor to Department of Business and Trade
·Jan 2024: Second patent awarded in US (pending in Europe, Japan, China, S. Korea)
·Jan 2024: DBT mission to **S. KOREA** and Intralink / meet strategic customers (Samsung)
·Mar 2024: Agreement with IIT Roorkee and Compact Modeling paper presented at IEEE-EDTM
·Mar 2024: **DBT mission to Axiom Space Houston US - ULTRARAM prj. NASA and Space Station**
·Apr 2024: Selected by InnovateUK for GBIP Semiconductors **TAIWAN** 2024 (x3)
·Apr 2024: Selected by UKBAA, Type One Ventures and UK Space Agency for their Venture into Space prog.
·*Jun 2024: Project launch (12 months): Industrial epitaxy scale-up of arrays/wafers with IQE. c£1m*
·Jul 2024: Unipolar Logic Device Field Effect Inverter: New patent filed, and academic paper prepared.
·Aug 2024: KAUST Saudi Arabia. Core Labs: Co-development of ALE Etching for InAs/AlSb.
·**Sept 2024: IC Taiwan Grand Challenge (ICTGC): Won prestigious internl prize, selected for >$3m investment.**
•Sept 2024: National Uni of Singapore: Collaboration to develop solutions for Neuromorphic/In-Memory Compute/EdgeAI

•Jan 2025: Pre-Seed round opens to raise £2M/$2.6M to fuel development of MVP's

Business Model

Innovation

We develop and iterate a universal memory roadmap

Manufacture

Market memories & EdgeAI chip in a range of form factors inc. wafer/die, chip and chiplet

License

To chip companies, OEMs and fabs

Revenues

From product, licensing, and royalties

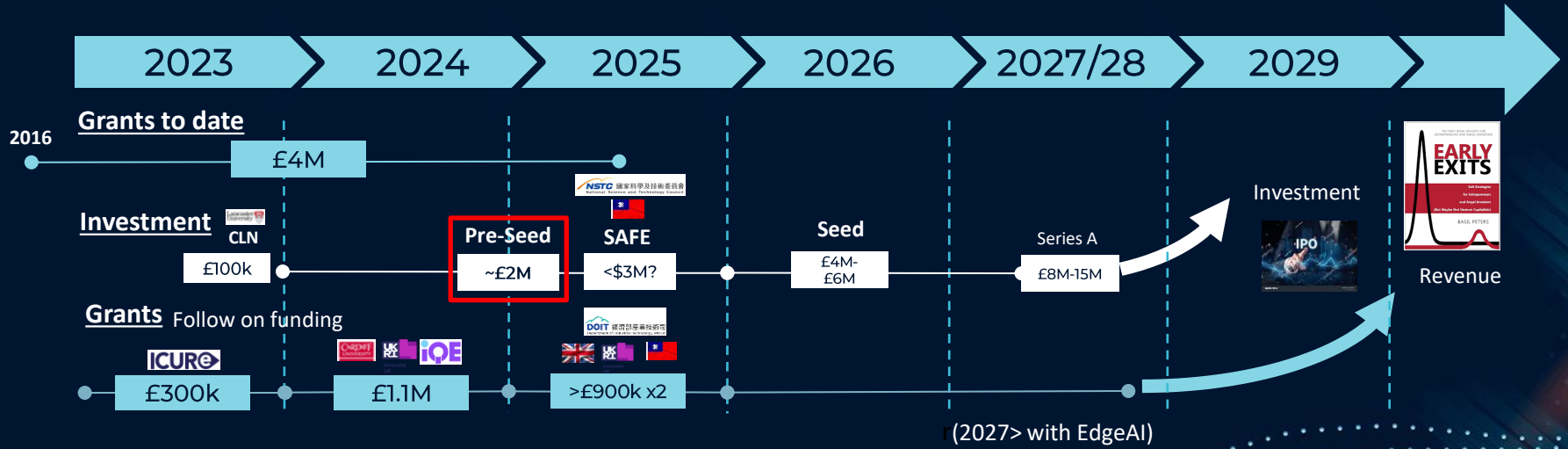
Revenue Streams:

- Product Sales: Direct sale of ULTRARAM™ chips and arrays for specific markets.
- Licensing and Royalties: Collaborations with semiconductor firms, fabs, and OEMs.
- Customized Solutions: Design and integration services for in-memory and neuromorphic computing.

Scaling Strategy:

- Partner with global fabrication and design houses to accelerate volume production.
- License IP to industry leaders in telecoms, AI, and IoT markets.

Funding Roadmap



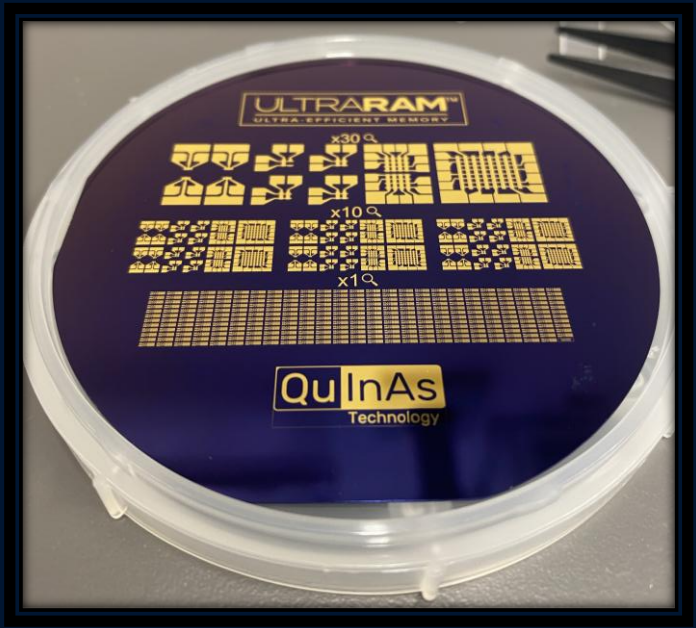
Funding Needs: Seeking investment for:

- Scaling R&D to complete TRL 5-6.
- Establishing pilot-scale production facilities (Taiwan).
- Building partnerships with global telecom and AI companies.

Collaboration Opportunities:

- Engage with advanced design houses for memory arrays.
- Partner with telecoms and AI companies to co-develop applications.
- Join forces with fabrication partners to enable scalable production.

Demo Wafer - 10µm Prototype



The demo wafer presents our prototype ULTRARAM™ memory devices at varying magnifications, illustrating their structure and **scalability**.

At **30× magnification** (top left), individual **single-bit devices** are visible, each featuring three contact pads linked by fine traces to the memory stack. To their right, **4-bit, 16-bit, and 64-bit memory arrays** are displayed, demonstrating increasing levels of **integration**.

Each cell within these arrays can be accessed for **read and write operations** by applying voltages to the respective **bit-lines and word-lines**, represented by the horizontal and vertical grid traces. By integrating each cell's **drain contact with a buried back-gate**, we have developed a **highly compact architecture**, significantly enhancing bit density.

Currently, we are fabricating **ULTRARAM™ with 10 µm feature sizes**, as shown at the bottom of the wafer. Our next milestone is a **100× reduction in size**, advancing to **100 nm devices** via **electron-beam lithography**, unlocking even greater scaling potential.

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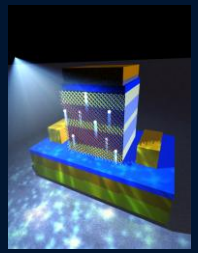
London W1W 7LT

R&D Labs

Physics Avenue
Lancaster LA1 4YB



Taiwan

Taipei Areana
Taipei City 105

Our Pre-Seed Round is now Open!

Join us to power the next revolution in computing

— and unlock a new era of energy-efficient memory for AI and beyond

Lancaster University