A Novel Scalable Array Design for III-V Compound Semiconductor-based Non-volatile Memory (UltraRAM) with Separate Read-Write Paths

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Abstract

The dream of achieving a *universal memory* that can provide robust non-volatile memory states along with low-energy operation has been the key driving force of memory research. Despite dominating the memory market, conventional charge-based memories cannot satisfy these requirements. However, UltraRAM, an oxide-free charge-based memory cell, aims to achieve both of these requirements. This device achieves non-volatility (with an endurance of over 10^7 cycles and a retention of over 1000 years) along with switching at low-voltage ($\pm 2.3\ V$) utilizing a triple-barrier resonant tunneling (TBRT) structure made of InAs/AlSb. In this work, we propose an array design for UltraRAM-based memory devices. Our proposed memory array features separate read-write path and eliminates the possibility of accidentally switching the memory states stored in the array. Moreover, our design allows us to read all the cells in a column in one cycle without imposing any limit on the scalability. Besides, since the read operation in our proposed design is independent of the write mechanism, there is flexibility to optimize the read operation for memory and in-memory computing applications.

Keywords

Array, Memory, Non-volatile memory, UltraRAM.

1. Introduction

Charge-based memories such as static random-access memory (SRAM), dynamic random-access memory (DRAM), and flash have dominated the memory market to date for both room temperature and cryogenic applications [1]–[3]. However, each of these memory technologies suffers from their own challenges. Flash memories are essentially metal-oxide-semiconductor field-effect transistors (MOSFETs) with a floating gate (FG) to store charge [4]. Storing/erasing charge in the FG determines the memory states and the non-volatile nature of the charge storage makes the flash memories suitable for data storage. However, to achieve this non-volatility, large voltage (typically $\pm 20\ V$ [5]) needs to be applied to the control gate (CG), which induces voltage-accelerated failure in the oxide separating FG and CG and consequently, limits the endurance of the flash memories [5], [6]. Compared to the flash memories, DRAMs can operate faster and with smaller voltages but suffer from destructive read [7]. Moreover, to preserve the data stored against the charge leaking from the capacitor, DRAMs need to be refreshed persistently (after every few tens of milli seconds). SRAM is the fastest among the charge-based memories and provides better data retention than DRAMs which makes SRAMs well suited for cache [8], [9]. However, the most efficient design of SRAM typically requires six transistors and, therefore, adhere to a large footprint to store one bit. Due to these issues, a number of emerging technologies (such as resistive [10], [11], spintronic [12], [13], ferroelectric [14], [15], phase change [16], etc.) have been explored in pursuit to find a *universal memory* [17].

A *universal memory* should feature fast speed, non-volatility, low voltage operation, low energy requirement, high endurance, high retention, high cost-efficiency to satisfy the memory requirements in different applications [17]. However, the apparently contradictory requirements of non-volatility and low energy (fast and low voltage operation) led to a conclusion that the realization of a *universal memory* is unrealistic if not impossible [1], [18]. However, in 2019, UltraRAM [19] was reported to achieve the contradictory requirement of non-volatility and low energy operation through a triple-barrier resonant tunneling (TBRT) structure using InAs quantum wells and AlSb barriers (Figure 1(a)). In UltraRAM, the memory states are defined by storing (erasing) the charge in (from) FG, alike the flash memories. However, the charges are stored in/erased from the FG of UltraRAM through the InAs/AlSb TBRT structure which has a conduction band offset of 2.1 eV. This barrier is larger than that of the flash memories (1.6 eV) which proves the non-volatility nature of the storage. Moreover, the device allows resonant tunneling at low voltages ($\pm 2.3\ V$). The combination of low voltage operation, non-volatility, and small capacitance leads to orders of magnitude lower switching energy compared to DRAMs and flash memories [20]–[22]. UltraRAM also provides large data retention of over 1000 years and high endurance of over 10^7 cycles [20].

Considering the immense prospects of UltraRAM, this can be a potential alternative to flash and DRAMs. However, to use any memory as data storage and active memory, the most important feature is to be able to access (write/read) any specific bit (cell) without disturbing other cells in the array. Also, the capability of scaling the memory to a larger size is of paramount importance. There is an existing design of UltraRAM memory array [21], [22] but the read operation in this array will face challenges (such as), when the size of the array is large and may even lead to a read failure in extreme cases. Therefore, the scalability of this design will be limited (discussed in section 3). In this work, we propose a novel

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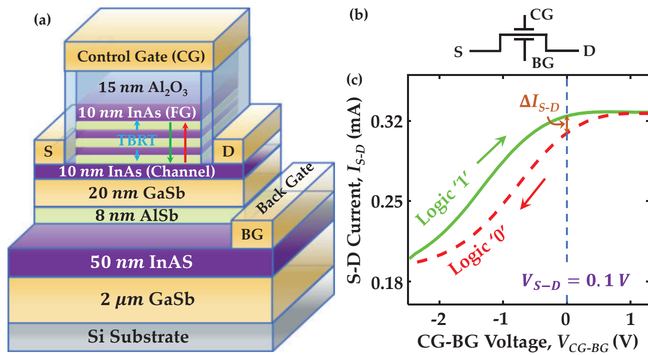

Figure 1:(a) Schematic and **(b)** symbol of the III-V semiconductor-based UltraRAM device. **(c)** Dependence of I_{S-D} on V_{CG-BG} and V_{S-D} which shows non-volatile memory states and low-voltage switching [20].

array structure for UltraRAM memories with separate read-write path capability which would not impose any limit on the scalability. Also, due to the use of separate read-write paths, the design provides high flexibility to optimize the read operation for different in-memory computing applications. The main contributions of this work are,

- Developing a circuit-compatible compact model for UltraRAM to facilitate circuit/system-level simulations,
- Investigating the existing array design and identifying the issues,
- Designing a novel array for UltraRAMs with separate read-write paths that do not impose any limit on the scalability of the array, and
- Demonstrating the operation of the proposed array through simulation.

The rest of the paper is organized as follows. Section 2 provides a brief background and operation of UltraRAM, Section 3 investigates the existing array design of UltraRAM and presents our proposed array and its advantages. Section 4 demonstrates the simulated read and write operations with our proposed array design, and Section 5 presents conclusions of the study.

(a)

Inputs

Variable Inputs
- Current State
- V_{CG-BG}
- V_{S-D}
- V_{S-D}^0

+

Constant Inputs
- $V_{CG-BG}^+ = 2.5\ V$
- $V_{CG-BG}^- = -2.5\ V$

State Update Module

if ($V_{CG-BG} \geq V_{CG-BG}^+$) *State = 1; else State = 0;*

State = 0

Current State?

State = 1

if ($V_{CG-BG} \leq V_{CG-BG}^-$) *State = 0; else State = 1;*

Parameter Selection

Choose Model Parameters ($A_1, A_2, V_{CG-BG}^0, dV$)

State = 0

Updated State?

State = 1

Choose Model Parameters ($A_1, A_2, V_{CG-BG}^0, dV$)

Output

$$I_{S-D} = \frac{V_{S-D}}{V_{S-D}^0} \times \left[\frac{A_1 - A_2}{1 + e^{\frac{V_{CG-BG} - V_{CG-BG}^0}{dV}}} + A_2\right]$$

(b) **Table for Choosing Model Parameters**

Parameters	State = 1	State = 0
A_1	0.19196	0.19259
A_2	0.32938	0.32979
V_{CG-BG}^0	-1.35027	-0.81267
dV	0.45746	0.47148

(c)

$V_{S-D} = 0.1\ V$

S-D Current, I_{S-D} (mA): 0.32, 0.25, 0.18

CG-BG Voltage, V_{CG-BG} (V): -3, -1.5, 0, 1.5, 3

Lines: Model
Dots: Experiment

Figure 2: (a) Overview of our approach to develop a compact model of UltraRAM. **(b)** List of the parameter values required to mimic the UltraRAM behavior with Boltzmann growth function. **(c)** Validation of our model with the experiment [20].

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2. Working principle and modeling of UltraRAM

In this section, we briefly discuss the structure, organization and features along with the modeling principles of UltraRAM.

Figures 1(a) and (b) show the schematic and symbol of the UltraRAM device, respectively. As seen in Figure 1(a), the device has four terminals- control gate (CG), back gate (BG), source (S), and drain (D). As mentioned earlier, the device stores the two logic states by storing (erasing) into (from) the floating gate which is separated from CG with an oxide (Al_2O_3) layer. FG stores logic '1' ('0') when the charges are erased from (trapped in) the FG. The channel of the device is made with an n-type InAs which determines the current separation between the two states. Between FG and the channel, multiple thin layers of InAs/AlSb are used to form the TBRT structure. Without any bias between CG and BG ($V_{CG-BG} = 0$), this structure does not allow any electron to pass to FG. However, upon applying a strong enough bias ($V_{CG-BG} \geq 2V$), electrons can be stored in FG (writing '0'). Similarly, applying a bias with opposite polarity ($V_{CG-BG} \leq -2V$), the stored electrons can be removed from FG (writing '1'). Therefore, to write into a memory cell, only a suitable bias between CG and BG is enough (Figure 1(c)).

Figure 1(c) shows the *I-V* characteristics of a UltraRAM device, where we can see that even when $V_{CG-BG} = 0$, there is enough separation between the currents of two logic states under a certain source-drain bias (V_{S-D}). This characteristic can be used for readout purpose. So, to read from a cell, only a suitable V_{S-D} needs to be applied keeping $V_{CG-BG} = 0$.

In this work, first, to facilitate the circuit/system level simulation using UltraRAM, we develop a Verilog-A-based compact model. Figure 2 shows the overview of our modeling approach. Here, we utilize the curve fitting tool of OriginLab software to mimic the *I-V* characteristics (separately for two states) shown in Figure 1(c). In this process, we use the Boltzmann growth function which is as follows-

$$f(x) = \frac{A_1 - A_2}{1+e^{\frac{x-x_0}{dx}}} + A_2 \quad (1)$$

Where, A_1, A_2, x_0, and dx are fitting parameters. Now, to mimic the dependence of the source-drain current (I_{S-D}) on V_{CG-BG} and V_{S-D}, we used a modified version of equation (1) which is as follow-

$$I_{S-D}(V_{CG-BG}, V_{S-D}) = \frac{V_{S-D}}{V_{S-D}^0} \times \left[\frac{A_1 - A_2}{1+e^{\frac{V_{CG-BG}-V_{CG-BG}^0}{dV}}} + A_2 \right] \quad (2)$$

Figure 2(b) shows the values of the fitting parameters of equation (2) for two states. After achieving a reasonable fit with this approach, we implement the model in Verilog-A to make this model capable of being used in the major circuit simulators such as SPICE, SPECTRE, etc. Figure 2(a) shows the steps of the modeling approach in Verilog-A. After getting the required inputs such as voltage biases, current state of the device, etc., the model compares V_{CG-BG} of the device with the suitable switching threshold and determines if the state will be changed or not. After that, with the updated state, the model chooses the values of the fitting parameters (listed in Figure 2(b)) and plugs the values into equation (2) which finally calculates the $I_{S-D}(V_{CG-BG}, V_{S-D})$. Figure 2(c) shows the validation of our developed model against the experimental data reported in [20].

3. Array design for UltraRAM memories

Scalability - capability of accessing individual cells in the array and preserving the stored information of the unaccessed cells from the accidental manipulation are the key characteristics that any memory device should possess for the practical use-cases. As a result, designing an array with all the above-mentioned characteristics is one of the most important tasks for any memory device. Figure 3(a) shows the schematic of the existing UltraRAM array reported in [21], [22]. In this array, the drain (D) contacts and BG contacts of all the UltraRAM devices are shorted together and serve as the common ground. Along the row (column), the CG (S) contacts of all the devices are connected together through word lines, WLs (bit lines, BLs). Now, to write into a memory cell, half of the write voltage ($\frac{V_{WRITE}}{2}$) is applied to the suitable WL (CG) and the other half is applied to the suitable BL (S) (Figure 3(b)). Upon applying these WL and BL biases, only the accessed cell gets V_{WRITE} as V_{CG-BG} and the cells in the same row and column of the accessed cell gets $\frac{V_{WRITE}}{2}$.

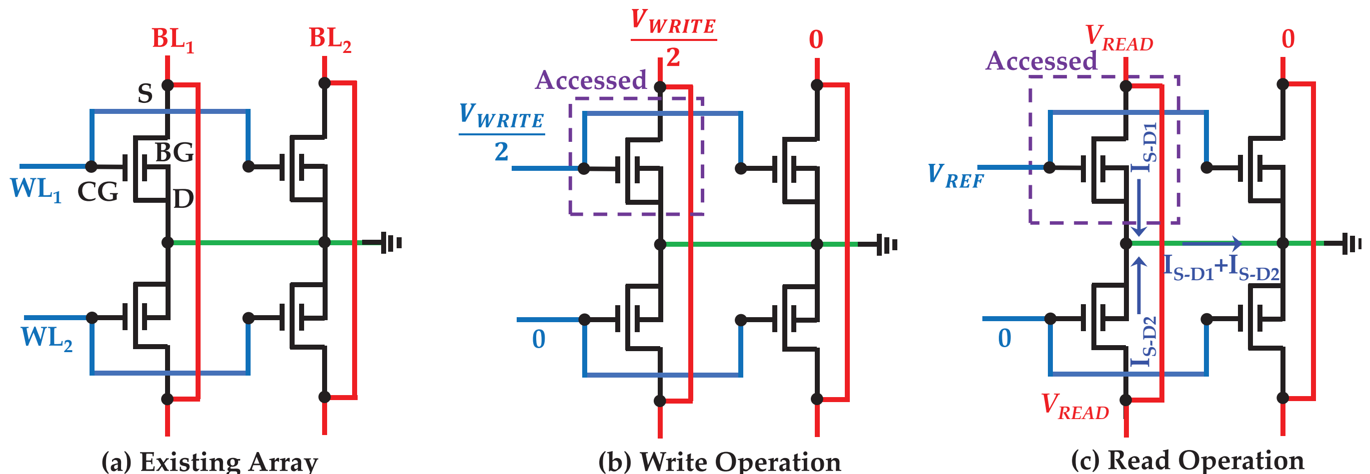

Figure 3: (a) Schematic of the existing array design for UltraRAM reported in [21], [22]. Mechanisms of **(b)** write and **(c)** read operations of a specific cell (marked with purple dashed box) in the array.

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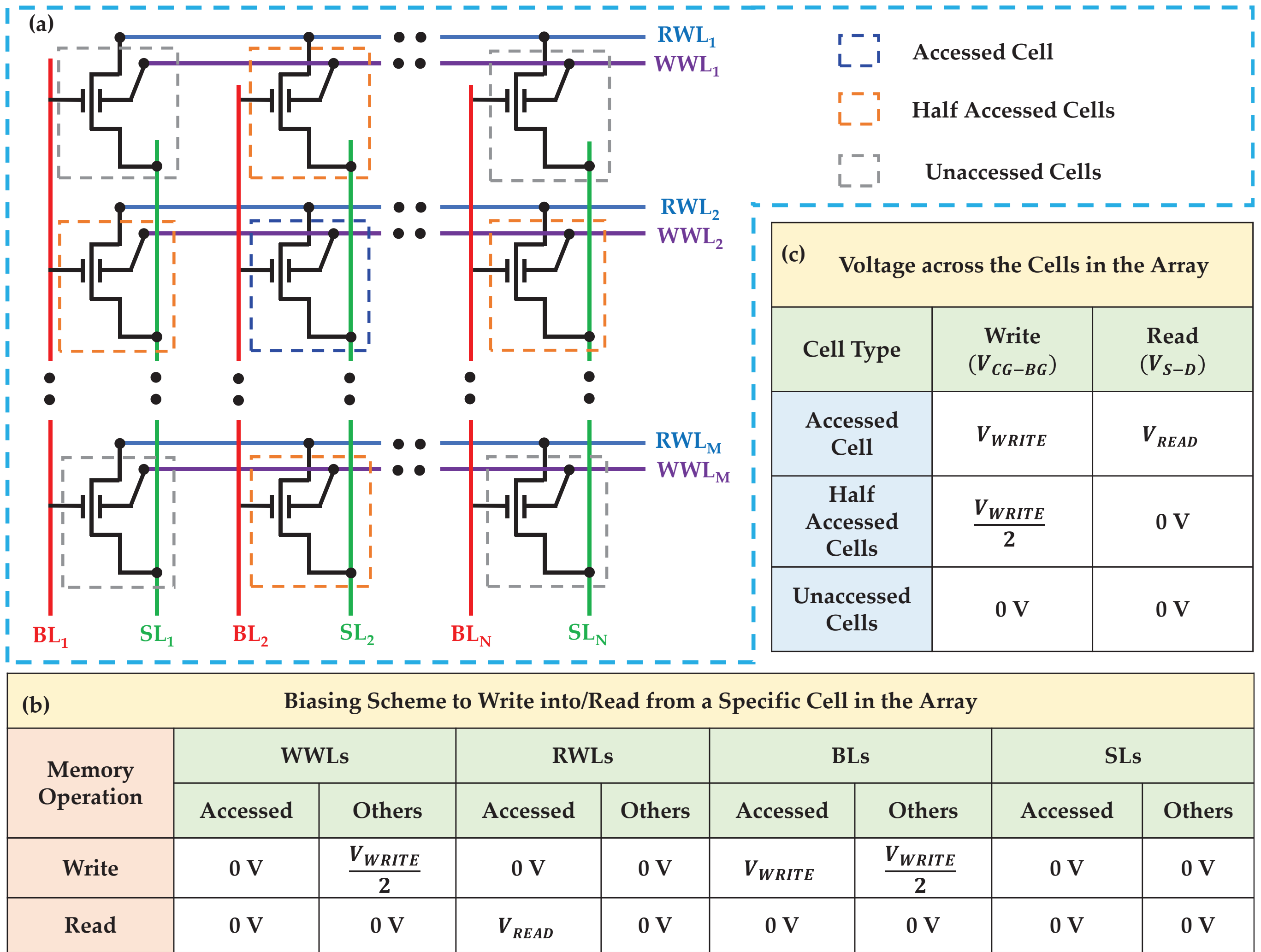

(c) Voltage across the Cells in the Array

Cell Type	Write (V_{CG-BG})	Read (V_{S-D})
Accessed Cell	V_{WRITE}	V_{READ}
Half Accessed Cells	$\frac{V_{WRITE}}{2}$	0 V
Unaccessed Cells	0 V	0 V

(b) Biasing Scheme to Write into/Read from a Specific Cell in the Array

Memory Operation	WWLs		RWLs		BLs		SLs	
	Accessed	Others	Accessed	Others	Accessed	Others	Accessed	Others
Write	0 V	$\frac{V_{WRITE}}{2}$	0 V	0 V	V_{WRITE}	$\frac{V_{WRITE}}{2}$	0 V	0 V
Read	0 V	0 V	V_{READ}	0 V	0 V	0 V	0 V	0 V

Figure 4: (a) Schematic of our proposed array design for UltraRAM memories. **(b)** Biasing scheme to write into and read from a specific cell (marked with blue box in (a)) in the proposed array. **(c)** V_{CG-BG} and V_{S-D} of accessed, half-accessed, and unaccessed (marked with blue, orange, and gray boxes in (a), respectively) cells during write and read operations, respectively.

Since, $\frac{V_{WRITE}}{2}$ cannot change the state of the memory cells, only the accessed cell gets written to the intended state. Now, for read operation, the shift in the threshold voltage (V_{TH}) corresponding to the device state is leveraged. Here, a voltage (V_{REF}) is first applied to the WL so that it only makes the cell storing logic '1' conducive (Figure 3(c)). For this, V_{REF} should be in between the two V_{TH} corresponding to two states. Then, a voltage is applied to the BL to get a current (I_{S-D}) based on the state stored in the accessed cell (Figure 3(c)). This design has been reported to work experimentally for a 2×2 array [22]. However, the read mechanism used in this design will limit the scalability of the array. For example, as shown in Figure 3(c), when we apply BL voltage to read from a specific cell, all the cells in the same column gets the same V_{S-D}. Even if other cells except the accessed one get $0\,V$ between their CG and BG, there should be a significant amount of I_{S-D} through these cells according to the characteristics shown in Figure 1(c) [20]. Also, as all the drain contacts in the array are tied together to ground, these I_{S-D} currents will be added to that of the accessed cell which will eventually lead to a read failure. Also, the currents that flow through the other cells in the column of the accessed cell depend on the state stored in those cells. This will necessitate more complicated peripheral circuit design and the choice of the reference to sense the memory state of the accessed cell.

To circumvent these issues of the existing array design, we propose a new array design for UltraRAM memories that allows the user to write into/read from any individual cell in the array using two separate paths and hence, without disturbance to other cells. Also, our proposed array and accessing technique does not impose any limitation on the scalability of the array. Figure 4(a) shows the schematic of our proposed array design. Unlike the existing array, in our design, we do not connect the BG and D contacts of the UltraRAM devices. Here, for write operations in any specific cell, we directly apply the write voltage between the CG and BG contacts of the cell through the BLs and write word lines (WWLs) but do not need any bias between the S and D contacts. And, for the read operation, we apply the read voltage between S and D contacts of the cell keeping $V_{CG-BG} = 0$. Here, the sense line (SL) current during read operation depends on the values of V_{S-D} and ΔI_{S-D} (marked

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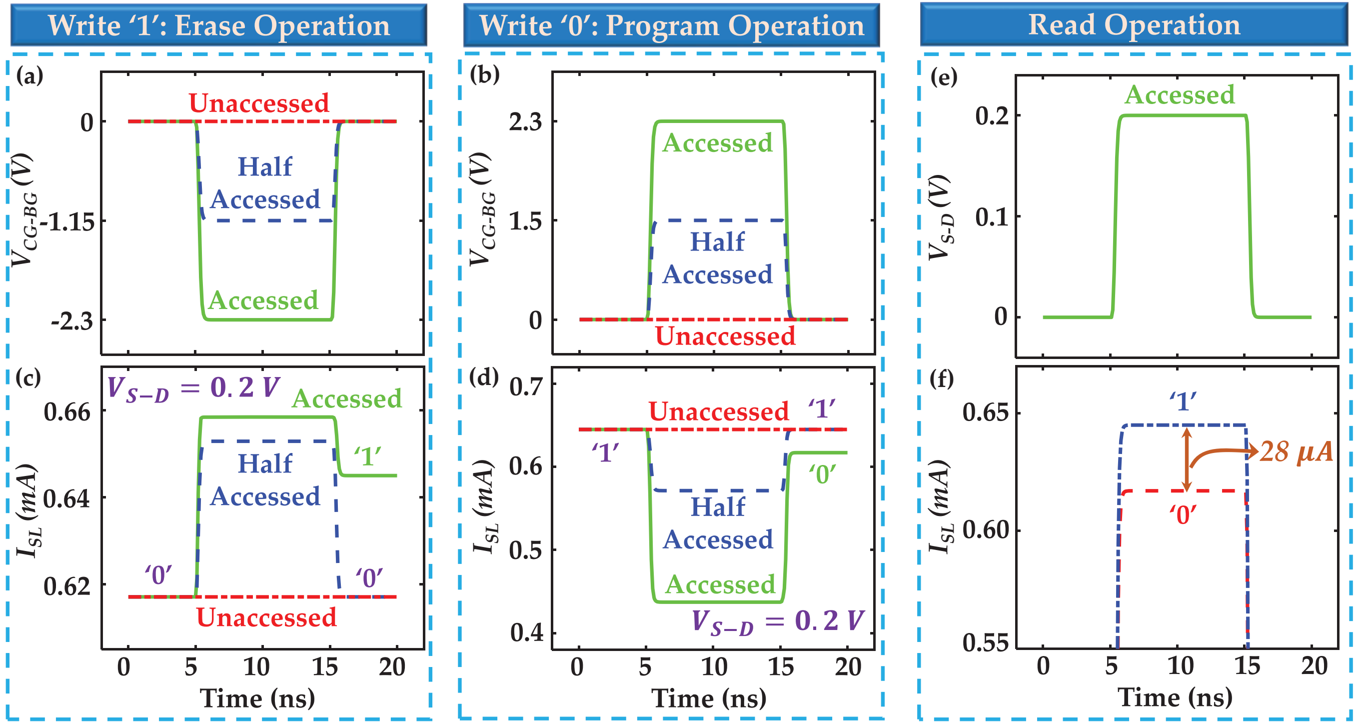

Figure 5: Applied V_{CG-BG} across the accessed, half-accessed, and unaccessed cells during **(a)** write ‘1’ and **(b)** write ‘0’ operations. SL currents with a V_{S-D} of 0.2 V for **(c)** write ‘1’ and **(d)** write ‘0’ operations. **(e)** Applied V_{S-D} across the accessed cell for read operation. **(f)** SL currents corresponding to the accessed cell storing logic ‘0’ and ‘1’. Note, our proposed memory array and biasing scheme allows the user to read all the cells in a column in a single cycle without causing any adverse impact.

in Figure 1(c)). The value of ΔI_{S-D} is crucial since it represents the sense margin and directly affects the read performance of the memory. One way to increase ΔI_{S-D} is to increase the applied V_{S-D} across the cell. However, in the existing design presented in Figure 3 (a), since both V_{CG-BG} and V_{S-D} are applied during read operation, the value of V_{S-D} must be less than $\frac{V_{WRITE}}{2}$ to prevent any accidental write. In our design, since we only use V_{S-D} to read from a cell in the array, we can use any value for V_{S-D} and hence, we can optimize the read performance to the fullest. As mentioned earlier, our proposed array uses two completely separate paths for write and read operations eliminating any possibility of accidental switching.

Figure 4(b) shows the biasing scheme to access (write into/read from) any specific cell in our proposed array. For ease of discussion, we assume that we want to access the (2, 2) cell in the array (marked with blue dashed box in Figure 4(a)). Now, to write into this cell, we utilize the $V/2$ biasing scheme [23], [24] for the BLs and WWLs. First, we apply V_{WRITE} ($\pm 2.3\ V$) to BL$_2$ and $\frac{V_{WRITE}}{2}$ ($\pm 1.15\ V$) to other BLs. Then, we apply 0 V to WWL$_2$ and $\frac{V_{WRITE}}{2}$ to other WWLs. These biases to BLs and WWLs make sure that the (2, 2) cell gets V_{WRITE}, the half-accessed cells (marked with orange dashed box in Figure 4(a)) get $\frac{V_{WRITE}}{2}$ (not enough to manipulate the state of the device), and the unaccessed cells (marked with orange dashed box in Figure 4(a)) get 0 V between the CG and BG contacts. Next, to read from the same cell, we apply V_{READ} to RWL$_2$ and 0 V to all the other control lines (RWLs, WWLs, BLs, and SLs). Due to this biasing, the accessed cell will get V_{READ} between the S and D contacts, and a current will flow through the corresponding SL based on the memory state stored in the cell. Note, our proposed array also allows to read from all the cells in one column in a single cycle without causing any issue since the cell currents will flow through separate SLs and hence, will be fed to separate sense amplifiers. Figure 4(c) shows the voltages dropped across the accessed, half-accessed and unaccessed cells during write and read operation of any specific cell in the array.

4. Simulated write and read operations

In our work, we adapt the simulation-based approach to demonstrate the memory operations in our proposed array. We discuss the simulated write and read operations in this section. Here, we simulate a 4×4 array in HSPICE. In the simulation framework, we utilize the developed Verilog-A-based compact model of UltraRAM device. First, we simulate the write operation. Figures 5(a) and 5(b) show V_{CG-BG} of the cells during write ‘1’ and ‘0’ operations, respectively resulting from the application of suitable biases to the WWLs and BLs. Note, during write ‘0’ (write ‘1’) operation before applying the biases, we initialize all the cells in logic ‘1’ (logic ‘0’) state. Now, to show that the intended write operations have been successfully performed, we apply a V_{S-D} of 0.2 V with the help of RWLs and SLs (not necessary to perform the write operation). For the same V_{S-D}, the cell storing logic ‘1’ leads to larger current flow than the cell storing logic ‘0’. Figures 5(c) and 5(d) show the SL currents (I_{SL}) corresponding to the accessed cell which show the successful ‘0’ → ‘1’ and ‘1’ → ‘0’ write operations,

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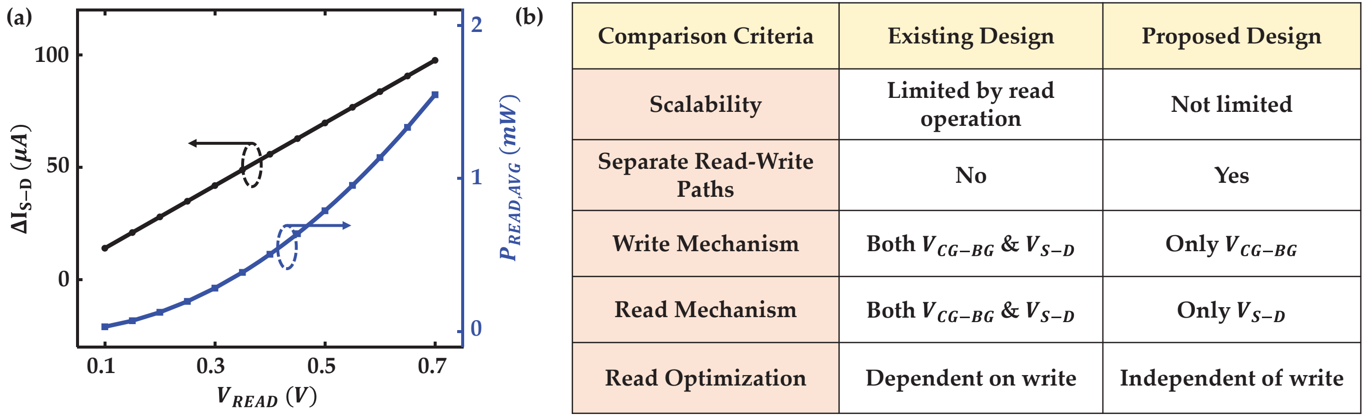

Comparison Criteria	Existing Design	Proposed Design
Scalability	Limited by read operation	Not limited
Separate Read-Write Paths	No	Yes
Write Mechanism	Both V_{CG-BG} & V_{S-D}	Only V_{CG-BG}
Read Mechanism	Both V_{CG-BG} & V_{S-D}	Only V_{S-D}
Read Optimization	Dependent on write	Independent of write

Figure 6: (a) Effects of V_{READ} on read distinguishability (ΔI_{S-D}) and average read power that can be leveraged to optimize the read operation. **(b)** Comparison of our proposed memory array with the existing design from [21], [22].

respectively. Figures 5(c) and 5(d) also show that the half-accessed cells get $\frac{V_{WRITE}}{2}$ between CG and BG but that cannot switch the state of the cell. Next, we simulate the read operation. Here, we apply V_{READ} between the suitable RWL and SL so that the accessed cell gets $V_{S-D} = V_{READ}$ (Figure 5(e)). As a result, the SL corresponding to the accessed cell shows two levels of current based on the state stored in that cell (shown in Figure 5(f)).

Here, we use $V_{READ} = 0.2\,V$ and we get a ΔI_{S-D} of $28\,\mu A$ which provides enough distinguishability to sense the memory states with a current-based sense amplifier [25], [26]. In our simulation, we measure an average read power of $1.26\,mW$ for $V_{READ} = 0.2\,V$. Next, we also simulate the read operations with different values of V_{READ} and show its effect on the average read power and the distinguishability (ΔI_{S-D}) in Figure 6 (a). Here, it is seen that increasing V_{READ} improves ΔI_{S-D} but leads to more power consumption. Note, unlike the existing design, our proposed array does not impose any limit on the value of V_{READ}. Therefore, our design provides more flexibility to optimize the write and read operations separately for other applications like in-memory computing. Figure 6(b) summarizes the improvements our design offers compared to the existing design.

4. Conclusion

UltraRAM memories offer a great potential to satisfy the contradictory requirement of robust non-volatile memory states and low energy operation of a *universal memory*. In this work, we proposed a novel memory array design for UltraRAM memory devices that uses two separate paths for write (CG and BG) and read (S and D) operations and hence, eliminates any possibility of accidental manipulation of the stored states. Moreover, our proposed design does not impose any limit on the scalability of the array as well as allows the user to read all the cells in a column in a single cycle without having any adverse impact on the performance. Finally, our design allows the use of any values of V_{READ} which facilitates the optimization of the read operation for memory and in-memory computing applications.

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